REMARKS

Applicant respectfully requests the Examiner's reconsideration of the present application as amended.

Claims 1-58, and 62-63 are pending in the present application.

Claims 1, 33, and 48 are rejected under 35 U.S.C. §101.

Claims 1-58, and 62-63 are rejected under 35 U.S.C. §102(b) as being unpatentable over U.S. Patent Publication 2001/0049814 ("Matsuoto").

Claims 1, 33, and 48 have been amended.

Support for amended claims 1, 33, and 48, is found on pages 4-28 of the specification, Figures 1-8(k) of the drawings, and claims 1-55 as originally filed. No new matter has been added.

Claims 1, 33, and 48 are rejected under 35 U.S.C. §101. The Office Action mailed 3/22/2007 states that

> [T]he claimed invention is directed to non-statutory subject matter. The act of the claimed expresses an abstract idea of selecting routing resources to increase delay for connection without specifies any data, functional, or practical application is non-statutory, see MPEP 2106 [R-3].

(3/22/2007 Office Action, p. 2)

Applicants submit that claims 1, 33, and 48 include subject matter that is statutory under 35 U.S.C. §101. Firstly, in State Street Bank & Trust Co. v. Signature Financial Group, Inc, 149 F.3d 1373, 1374 (Fed. Cir. July, 1998), the Court of Appeals for the Federal Circuit held that "transformation of data, representing discrete dollar amounts, by a machine through a series of mathematical calculations into a final share price constitutes a practical application ... ... because it produces 'a useful, concrete, and tangible result'". Applicants respectfully submit that determining minimum and maximum delay budgets for connections along a path by finding a set of connection delays that satisfy short-path and long-path timing constraints for the path, and selecting routing resources for implementing the connections in the system in response to

Serial No. 10/774,857   10   ALT.P027.1(A1182.1)

the minimum and maximum delay budgets as described in claims 1, 33, and 48 similarly

represent statutory subject matter under 35 U.S.C. § 101. The determination of minimum and

maximum delay budgets for the connections, and selection of routing resources for the system in

response to the determined minimum and maximum delay budgets are thus also practical

applications that produce a "useful, concrete, and tangible result".

Secondly, applicants submit that the routing resources selected for implementing the

connections in the system recited in claims 1, 33, and 48 represent physical objects. The Federal

Circuit Court of Appeals has ruled that the manipulation of data representing physical objects or

activities, where the data comprises signals corresponding to physical objects or activities

external to the computer system and the process causes a physical transformation of the signals

which are intangible representation of the physical objects or activities, constitutes a statutory

process (see In re Schrader 22 F.3d 290, 294 (Fed. Cir. 1994) and Arrhythmia Research Tech. v.

Corazonix Corp, 958 F.2d 1053, 1058-1059 (Fed. Cir. 1992) and also MPEP 2106, p. 2100-16

(Rev. 3 August 2005) which states that the subject matter constitutes a safe harbor for being

statutory).

Thirdly, applicants submit that "selecting routing resources for implementing the

connections in the system in response to the minimum and maximum delay budgets" recited in

claims 1, 33, and 48 represent a practical application by physical transformation. MPEP 2106

IV.C. 2. states that

> A claimed invention is directed to a practical application of a 35
> U.S.C. 101 judicial exception when it: (A) "transforms" an
> article or physical object to a different state or thing;

(MPEP 2106 IV.C.2, p 2100-11 (Rev. 5 Aug. 2006).

Applicants submit that the "system" is an article or physical object that is "transformed"

by the selection of "routing resources". Thus, applicants submit that MPEP 2106 IV.C. 2. (1)

requires that if "USPTO personnel find such a transformation or reduction, USPTO personnel

shall end the inquiry and find that the claim meets the statutory requirement of 35 U.S.C. 101."

Serial No. 10/774,857   11   ALT.P027.1(A1182.1)

For at least these reasons, the claims are deemed to define statutory subject matter.

Applicants submit that in view of the state of the law summarized above, claims 1, 33, and 48 are patentable under 35 U.S.C. §101.

The Examiner has rejected claims 1-58, and 62-63 under 35 U.S.C. §102(b) as being anticipated by Matsuoto. In particular, the Examiner has stated that

> As to claims 1, and 33, Matsuoto et al. teaches a method for designing a system, comprising: determining minimum and maximum delay budgets for connections along a path by finding a set of connection delays that attempt to satisfy the short-path (see fig 8) and long-path (see fig 9) timing constraints for the path (see fig 8 Fig. 9, paragraph 0089-00125); and selecting routing resources for the connections in response to the minimum and maximum delay budgets (see fig 1, fig 8, fig 9 element 104, 0082-0088 and 00126-0131).

(3/22/2007 Office Action, pp. 2-3)

As stated above, claims 1, 33, and 48 have been amended.

It is submitted that Matsuoto does not render claims 1-58, and 62-66 unpatentable under 35 U.S.C. §102(b).

Matsuoto includes a disclosure of a method and apparatus capable of laying out a circuit of logic synthesis result so as to be able to satisfy delay constraints without changing the logic structure. For this reason, one solution means is to provide a layout program controlling information unit including a cell grouping process for placing a plurality of cells within a logic circuit in a logic circuit obtained by processing through the use of a logic synthesis unit to be adjacent to each other, and generating an adjacent placement instruction for realizing wiring between cells made adjacent to each other in local inter-connect, and a wire length budgeting process for giving a wire length budget to nets within the logic circuit so as to be able to satisfy delay constraints. In the layout process, placement and routing will be performed in accordance with these adjacent placement instruction and wire length budget. Thereby, re-design of the

Serial No. 10/774,857   12   ALT.P027.1(A1182.1)

previous process of the design can be avoided to reduce the number of design man-hour of LSI
(see Matsuoto Abstract).

It is submitted that Matsuoto does not disclose determining minimum and maximum
delay budgets for connections along a path by finding a set of connection delays that satisfy
short-path and long-path timing constraints for the path, and selecting routing resources for
implementing the connections in the system in response to the minimum and maximum delay
budgets.

On the contrary, Matsumoto discloses a wire length budgeting process where a procedure
for giving a short wire length is used to give a short wire length to a net on a severe delay path
(see Matsumoto [0087]-[0107] and Figure 8) and a procedure for giving a long wire length is
based on giving long wire lengths to "remaining net(s)" that are not on a severe delay path (see
Matsumoto [0088], [0108]-[0120] and Figure 9). The procedures for giving short wire lengths
and long wire lengths are not related to meeting short-path timing constraints. The wire length
budgeting process described in Matsumoto gives a wire length budget to a net in the logic circuit
to lay out in such a manner that the layout process becomes equal to or less than the wire length
given to the net (see Matsumoto [0011]). The wire length budgeting process described in
Matsumoto does not satisfy a short-path timing constraint which indicates that the delay from
one end of the path to the other must be no smaller than a defined value.

In contrast, claim 1 states

> A method for designing a system, comprising:
> determining minimum and maximum delay budgets for
> connections along a path by finding a set of connection delays
> that satisfy a short-path timing constraint for the path, which
> indicates that the delay from one end of the path to an other end
> must be no smaller than a first value, and a long-path timing
> constraint for the path, which indicates that the delay from one
> end of the path to the other end must be no larger than a second
> value; and
> selecting routing resources for implementing the connections
> in the system in response to the minimum and maximum delay
> budgets.

(Claim 1) (Emphasis Added).

Claims 33 and 48 include similar limitations of determining minimum and maximum delay budgets for connections along a path from long-path and short-path timing constraints. Given that claims 2-32, 52-58, and 62-63 depend from claim 1, claims 34-47 depend from claim 33, and claims 49-51 depend from claim 48, it is likewise submitted that claims 2-32, 34-47, 49-58, and 62-63 are also patentable under 35 U.S.C. §102(b) over Matsumoto.

It is submitted that Matsumoto does not disclose determining minimum and maximum delay budgets for the connections by allocating short-path and long-path slack.

The Examiner cites Figures 8 and 9, and paragraphs [0089]-[0125] as evidence that Matsumoto discloses "determining minimum and maximum delay budgets for the connections comprises allocating short-path and long-path slack" (3/22/07 Office Action, p. 4). Applicants submit that the cited sections by the Examiner do not disclose the allocation of short-path or long-path slack to establish minimum and maximum delay budgets used for selecting routing resources. In fact, Applicants could not find any disclosure or mention of short-path and long-path slack in the entire Matsumoto reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 8 unpatentable.

In contrast, claim 8 states

> The method of Claim 1, wherein determining minimum and maximum delay budgets for the connections comprises allocating short-path and long-path slack.

(Claim 8) (Emphasis added).

Claim 40 includes similar limitations. Given that claims 9-18 and claims 41-42 depend directly or indirectly on claims 8 and 40, it is likewise submitted that claims 9-18 and 41-42 are also patentable under 35 U.S.C. §102(b) over Matsumoto.

It is submitted that Matsumoto does not disclose re-selecting routing resources for connections that are shorted.

Serial No. 10/774,857   14   ALT.P027.1(A1182.1)

The Examiner cites Figures 1, 8, and 9 and paragraphs [0082]-[0088], [0126]-[0131], and the summary as evidence that Matsumoto discloses "wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises re-selecting the routing resources for connections that are shorted" (3/22/07 Office Action, p. 6). Applicants submit that the cited sections by the Examiner do not disclose re-selecting routing resources for connections that are shorted. In fact, applicants could not find any disclosure or mention of shorted connections in the entire Matsumoto reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 20 unpatentable.

In contrast, claim 20 states

> The method of Claim 1, wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises re-selecting the routing resources for connections that are shorted.

(Claim 20) (Emphasis added).

Claim 44 includes similar limitations.

It is submitted that Matsumoto does not disclose either decreasing minimum delay budgets based on the number of routing iterations that have occurred or increasing maximum delay budgets based on the number of routing iterations that have occurred.

The Examiner cites Figures 1, 8, and 9, and paragraphs [0082]-[0088], and [0126]-[0131] as evidence that Matsumoto discloses "decreasing minimum delay budgets based on the number of routing iterations that have occurred" and "increasing maximum delay budgets based on the number of routing iterations that have occurred" (3/22/07 Office Action, p. 6). Applicants submit that the cited sections by the Examiner do not disclose decreasing minimum delay budgets based on the number of routing iterations that have occurred or increasing the maximum delay budgets based on the number of routing iterations that have occurred. In fact, applicants could not find any disclosure or mention of routing iteration in the entire Matsumoto reference.

Serial No. 10/774,857   15   ALT.P027.1(A1182.1)

Applicants respectfully request the Examiner to clarify how the cited text render claims 21 and 22 unpatentable.

In contrast, claim 21 states

> The method of Claim 1, wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises decreasing minimum delay budgets based on the number of routing iterations that have occurred.

(Claim 21) (Emphasis added).

Claim 45 includes similar limitations.

Claim 22 states

> The method of Claim 1, wherein selecting routing resources for connections in response to the minimum and maximum delay budgets comprises increasing maximum delay budgets based on the number of routing iterations that have occurred.

(Claim 22) (Emphasis added).

Claim 46 includes similar limitations.

It is submitted that Matsumoto also does not disclose short-path timing constraints that comprises a hold time requirement.

The Examiner cites Figures 8 and 10, and paragraphs [0091]-[0107] as evidence that Matsuoto discloses "wherein the short-path timing constraints comprises a hold time requirement" (3/22/2007 Office Action, p. 9). Applicants submit that the cited sections by the Examiner do not disclose a short-path timing constraint that comprises a hold time requirement. In fact applicants could not find any disclosure or mention of hold time requirements in the entire Matsuoto reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 56 unpatentable.

In contrast, claim 56 states

> The method of Claim 1, wherein the short-path timing constraints comprises a hold time requirement.

(Claim 56) (Emphasis Added).

Serial No. 10/774,857   16   ALT.P027.1(A1182.1)

It is submitted that Matsuoto also does not teach or suggest short-path timing constraints that comprises a minimum propagation delay.

The Examiner cites Figures 8 and 10, and paragraphs [0091]-[0107] as evidence that Matsuoto discloses "wherein the short-path timing constraints comprises a minimum propagation delay" (3/22/2007 Office Action, p. 9). Applicants submit that the cited sections by the Examiner do not disclose a short-path timing constraint that comprises a minimum propagation delay. In fact, applicants could not find any disclosure or mention of a minimum propagation delay in the entire Matsuoto reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 57 unpatentable.

In contrast, claim 57 states

> The method of Claim 1, wherein the short-path timing constraints comprises a minimum propagation delay.

(Claim 57) (Emphasis Added).

It is submitted that Matsuoto also does not teach or suggest short-path timing constraints that comprises a minimum clock-to-output requirement.

The Examiner again cites Figures 8 and 10, and paragraphs [0091]-[0107] as evidence that Matsuoto discloses "wherein the short-path timing constraints comprises a minimum clock-to-output requirement" (3/22/2007 Office Action, p. 9). Applicants submit that the cited sections by the Examiner do not disclose a short-path timing constraint that comprises a minimum clock-to-output requirement. In fact, applicants could not find any disclosure or mention of a minimum clock-to-output requirement in the entire Matsuoto reference. Applicants respectfully request the Examiner to clarify how the cited text renders claim 58 unpatentable.

In contrast, claim 58 states

> The method of Claim 1, wherein the short-path timing constraints comprises a minimum clock-to-output requirement.

(Claim 58) (Emphasis Added).

Serial No. 10/774,857   17   ALT.P027.1(A1182.1)

In view of the arguments set forth herein, it is respectfully submitted that the applicable rejections and have been overcome. Accordingly, it is respectfully submitted that claims 1-58, and 62-63 should be found to be in condition for allowance.

If any additional fee is required, please charge Deposit Account No. 50-1624.

Respectfully submitted,

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